Notice of Allowability	Application No.	Applicant(s)	
	10/759,027	SHIH, PO-SHENG	
	Examiner	Art Unit	
	David Nhu	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *8/4/04*.

2. ☒ The allowed claim(s) is/are *1-20*.

3. ☒ The drawings filed on *20 January 2004* are accepted by the Examiner.

4. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☒ Certified copies of the priority documents have been received in Application No. *10/395,169* .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

REASONS FOR ALLOWANCE

1. Claims 1-20 are allowed.

2. The following is an examiner's statement of reasons for allowance: None of the references of record teaches or suggests as cited in claims 1, 15, 20: forming a common line and a data line extending longitudinally on the gate insulation layer, and forming a source electrode and a drain electrode on the semiconducting island to form a thin transistor (TFT) structure, wherein the drain electrode electrically connects the data line; forming a first via hole and a second via hole penetrating the dielectric layer and the planrization layer, wherein the first via hole exposes a surface of the source electrode, and the second via hole exposes part of a surface of the first conductive layer and part of a surface of the common line; forming a conformal second conductive layer on the dielectric layer, an interior surrounding surface of the first via hole and an inter surrounding surface of a second via hole (as cited in claim 1); forming a common line and a data line extending longitudinally on the gate insulation layer, and forming a source electrode and a drain electrode on the semiconducting island to form a thin transistor (TFT) structure, wherein the drain electrode electrically connects the data line; forming a first via hole and a second via hole penetrating the dielectric layer and the planrization layer, wherein the first via hole exposes a surface of the source electrode, and the second via hole exposes part of a surface of the first conductive layer and part of a surface of the common line, and the second via hole and the first opening have an overlap; forming a conformal second conductive layer on the dielectric layer, an interior surrounding surface of the first via hole and an inter surrounding surface of a second via hole; removing part of the second conductive layer to form a third conductive layer, a fourth conductive layer, and a second opening,

wherein the third conductive layer is isolated from the fourth conductive layer by the second opening (as cited in claim 15); using a third mask to form a common line and a data line longitudinally extending on the gate insulation layer by photolithography, and forming a source electrode and a drain electrode on the semiconducting island to form a thin transistor structure, wherein the drain electrode electrically connects the date line; using a fifth mask to form a first via hole and a second via hole penetrating the dielectric layer and the planrization layer, wherein the first via hole exposes a surface of the source electrode, and the second via hole exposes part of a surface of the first conductive layer and part of a surface of the common line; forming a conformal second conductive layer on the dielectric layer, an interior surrounding surface of the first via hole and an inter surrounding surface of a second via hole; using a sixth mask to remove part of the second conductive layer to form a third conductive layer, a fourth conductive layer and a first opening by photolithography, wherein the third conductive layer is isolated from the fourth conductive layer by the firs opening; wherein the first conductive layer electrically connects the common line by the fourth conductive layer (as cited in claim 20)

4. Applicants filed an amendment on 7/26/04, and also filed at that time **a terminal disclaimer statement with reference to USP: 6,723,592 B2.**

5. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

CONCLUSION

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure: Shih (6,723,592 B2): Method of Fabricating a X-Ray Detector Array Elements.

7. Any inquiry concerning this communication on earlier communications from the examiner should be directed to David Nhu , (571)272-1792. The examiner can normally be reached on Monday-Friday from 7:30 AM to 5:00 PM.

The examiner's supervisor, David Nelms can be reached on (571)272-1787.

The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956

David Nhu DN

August 23, 2004

DAVID NHU
PRIMARY EXAMINER